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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,919	03/26/2004	Tsunehiro Hato	040156	6752
23850 75	90 11/29/2005		EXAM	INER
ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP 1725 K STREET, NW SUITE 1000			PHAM, LONG	
			ART UNIT	PAPER NUMBER
WASHINGTON	N, DC 20006		2814	
			D. (772) (1172) (1172) (1772)	-

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)			
	10/809,919	HATO ET AL.			
Office Action Summary	Examiner	Art Unit			
	Long Pham	2814			
The MAILING DATE of this communication Period for Reply	n appears on the cover sheet v	vith the correspondence address			
A SHORTENED STATUTORY PERIOD FOR R WHICHEVER IS LONGER, FROM THE MAILIN - Extensions of time may be available under the provisions of 37 C after SIX (6) MONTHS from the mailing date of this communicati - If NO period for reply is specified above, the maximum statutory - Failure to reply within the set or extended period for reply will, by Any reply received by the Office later than three months after the earned patent term adjustment. See 37 CFR 1.704(b).	NG DATE OF THIS COMMUN FR 1.136(a). In no event, however, may a on. period will apply and will expire SIX (6) MO statute, cause the application to become A	ICATION. Treply be timely filed NTHS from the mailing date of this communication. ABANDONED (35 U.S.C. § 133).			
Status					
1) Responsive to communication(s) filed on	•				
·— ·	This action is non-final.				
3) Since this application is in condition for all					
Disposition of Claims					
4) ⊠ Claim(s) <u>1-17</u> is/are pending in the applic 4a) Of the above claim(s) <u>11-17</u> is/are with 5) ☐ Claim(s) is/are allowed. 6) ⊠ Claim(s) <u>1-7</u> is/are rejected. 7) ⊠ Claim(s) <u>8-10</u> is/are objected to. 8) ☐ Claim(s) are subject to restriction and	hdrawn from consideration.				
Application Papers	·				
9) ☐ The specification is objected to by the Exa	aminer.				
10) The drawing(s) filed on is/are: a)] accepted or b)☐ objected to	by the Examiner.			
Applicant may not request that any objection to	to the drawing(s) be held in abeya	ance. See 37 CFR 1.85(a).			
Replacement drawing sheet(s) including the call 11) The oath or declaration is objected to by the call to be a second sec					
Priority under 35 U.S.C. § 119					
12) Acknowledgment is made of a claim for for a) All b) Some * c) None of: 1. Certified copies of the priority docu 2. Certified copies of the priority docu 3. Copies of the certified copies of the application from the International B * See the attached detailed Office action for	ments have been received. ments have been received in a e priority documents have bee dureau (PCT Rule 17.2(a)).	Application No n received in this National Stage			
Attachment(s) 1) ☑ Notice of References Cited (PTO-892)	4) 🗆 Interview	Summary (PTO-413)			
 Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-94) Information Disclosure Statement(s) (PTO-1449 or PTO/92) Paper No(s)/Mail Date 09/15/04. 	18) Paper No	o(s)/Mail Date Informal Patent Application (PTO-152)			

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DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-10 in the reply filed on 09/20/05 is acknowledged.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in combination with Adachi et al. (US publication 2004/0077504).

With respect to claim 1, AAPA teaches a superconducting circuit comprising (see the Description of Related Art of this application):

A single flux quantum circuit using a high temperature superconductor; and An interface circuit for said single flux quantum circuit, wherein said single flux quantum circuit is provided with a first superconductor or josephson junction and said interface circuit is provided with a second superconductor or josephson junction.

AAPA further teaches that the superconductor or josephson junction of the single flux quantum circuit requires small hysteresis in the current-voltage characteristic and the superconductor or josephson junction of the interface circuit

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requires hysteresis in the current-voltage characteristic but fails to teach obtaining the desired current-voltage characteristics or hysteresis of the superconductor or josephson junction of the single flux quantum circuit and the superconductor or josephson junction of the interface circuit by changing materials of the junctions or using different materials for the junctions.

Adachi et al. teach that the desired current-voltage characteristics or hysteresis of superconductor or josephson junctions can be obtained by using different material for the junctions. See [0048] to [0060].

It would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to use different materials for the junctions to achieve different current-voltage characteristics or hysteresis in the device of AAPA to allow the formation of single flux quantum circuit and interface circuit.

With respect to claim 2, AAPA further teaches the interface circuit is formed of latch driver circuit. See the Background of the invention of this application.

With respect to claims 3 and 4, AAPA and Adachi et al. fail to teach the ranges for the percent of the hysteresis for the first and second josephson junctions.

However, it would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to determine the workable or optimal value or range for the percent of hysteresis for the first and second junctions through routine experimentation and optimization to obtain optimal or desired device performance because in the absence of unexpected results it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claims 5, 6, and 7, AAPA fails to teach the first and second josephson junctions

Adachi et al. teach using ramp edge junctions because its high driving capability during switching operation. See [0006].

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It would have been obvious to one of <u>ordinary skill</u> in the art of making semiconductor devices to incorporate the teachings of Adachi et al. into the device of AAPA to obtain the above benefit.

Allowable Subject Matter

Claims 8-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ľong **P**ham

Primary Examiner

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